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EFS ID: 22182
Application ID: 09596382
Title of Invention: A PROCESS FOR
MANUFACTURING AN
INTEGRATED CIRCUIT INCLUDING
A DUAL-DAMASCENE STRUCTURE
AND A CAPACITOR
First Named Inventor: Sailesh Chittipeddi
Domestic/Foreign Application: Domestic Application
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Electronic Information Disclosure Statement

A PROCESS FOR MANUFACTURING AN INTEGRATED CIRCUIT INCLUDING A DUAL-DAMASCENE STRUCTURE AND A CAPACITOR


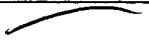

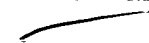
Application: 
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Applicant(s): Sailesh Chittipeddi
Docket Number: CHITTIPEDDI
Group Art Unit: 2812
Examiner: H. Jey Tsai
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01 FC:1806 180.00 CH

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Citation No.	Patent Number	Date	Bar Code	Patentee	Class	Subclass
	P01	6037216	2000-03-14		Liu et al.	438	253
	P02	5633781	1997-05-27		Saenger et al.	361	321.4

Signature

Examiner Name	Date
Ch. Joe TSM	6/22/03